WHAT IS CLAIMED IS:

1. A system for testing an integrated circuit, comprising:

a random bit generator adapted to produce a random pattern of bits, at least a portion of which are configured to be clocked in parallel onto n conductors at a first rate; and

logic adapted to compare each of the random pattern of bits with each of the random pattern of bits after having been converted to a serial bit stream clocked at a second rate equal to *n* times the first rate.

2. The system as recited in claim 1, wherein the generator produces a random pattern of *m* bits.

3. The system as recited in claim 2, wherein the logic further comprises:

a frame compile circuit for gathering frames of *m* bits from the serial bit stream;

a second random bit generator adapted to produce a second random pattern of bits identical to the random pattern of bits; and

a comparator coupled to the frame compile circuit and the second random bit generator to receive the frames of *m* bits and compare each bit within the frames of *m* bits to respective bits within the second random pattern of bits.

4. The system as recited in claim 3, further comprising a latch coupled to an output of the comparator for storing a signal indicating failure of a serializer which converts the random pattern of bits to the serial bit stream if each bit of frames of *m* bits are not at the same logic level as respective *m* bits of the second random pattern of bits.

5. The system as recited in claim 3, further comprising:

a deserializer which converts the serial bit stream to at least one parallel-delivered set of *n* bits placed onto another set of *n* conductors at the second rate divided by *n*; and

a latch coupled to an output of the comparator for storing a signal indicating failure of the deserializer if each bit of the frames of *m* bits, after having undergone deserialization, are not at the same logic level as respective *m* bits of the second random pattern bits.

6. The system as recited in claim 1, further comprising a test access port adapted to receive an instruction compliant with IEEE Std. 1149.1, and to present the instruction to the generator for signaling production of the random pattern of bits.

7. The system as recited in claim 1, wherein the instruction is forwarded from a host computer operating from an application program compatible with IEEE Std. 1149.1.

8. The system as recited in claim 7, wherein the application program comprises the JAM™ Standard Test and Programming Language (STAPL).

9. A self-test circuit, comprising:

a serializer having an input and an output, wherein the input is coupled to receive a random pattern of *m* bits clocked in parallel upon *n* conductors at a first rate, and wherein the output is coupled to produce a serial bit stream clocked at *n* times the first rate;

a deserializer coupled to receive the serial bit stream via a loop back conductor selectably connected between the serializer and the deserializer; and

a comparator coupled to receive *m* bits from the deserializer and to compare each of the *m* bits from the deserializer to corresponding bits identical to the random pattern of *m* bits placed on the input of the serializer for testing the serializer and the deserializer.

10. The self-test circuit as recited in claim 9, further comprising:

a clock generator coupled to selectively forward a first clock transitioning at the first rate to the serializer for synchronously receiving the random pattern of *m* bits; and

a first phase-locked loop coupled to receive the first clock and to multiply the first rate by *n* to form a second clock transitioning at a second rate for clocking the serial bit stream.

11. The self-test circuit as recited in claim 9, further comprising at least one relay coupled to selectively connect the loop back conductor between the serializer and the deserializer.

12. The self-test circuit as recited in claim 9, wherein the serializer comprises a transmit circuit coupled to accept the random pattern of *m* bits and transmit the serial bit stream, and wherein the deserializer comprises a receive circuit coupled to receive the serial bit stream and produce a plurality of frames consisting of *m* bits.

13. The self-test circuit as recited in claim 12, wherein the transmit circuit includes a phase locked loop having a divide-by *n* counter within a feedback loop of the phase locked loop.

14. The self-test circuit as recited in claim 12, wherein the receive circuit includes a phase locked loop having a multiply-by *n* counter within a feedback loop of the phase locked loop.

15. The self-test circuit as recited in claim 9, wherein the serializer, the deserializer, and the comparator are interconnected upon a single printed circuit board.

16. The self-test circuit as recited in claim 9, wherein the serializer, the deserializer, and the comparator are interconnected upon a single semiconductor substrate.

17. The self-test circuit as recited in claim 9, wherein at least a portion of the serializer, the deserializer, and the comparator comprise a programmable logic device.

18. The self-test circuit as recited in claim 9, wherein the *m* bits from the deserializer are arranged in a sequence identical to the *m* bits clocked in parallel upon the *n* conductors of the serializer such that the comparator compares the first bit within the sequence from the deserializer with respective bits within the random pattern of *m* bits.

19. A method for testing a serializer circuit and a deserializer circuit, comprising:

generating a random pattern of bits;

forwarding the random pattern of bits at a first rate;

serializing the random pattern of bits into a serial bit stream at a second rate;

deserializing the random pattern of bits at the first rate;

comparing each bit within the random pattern of bits with respective bits within the deserialized random pattern of bits to determine functional failure of the serializer and deserializer.

20. The method as recited in claim 19, wherein said forwarding the random pattern of bits comprises clocking the bits in parallel upon n conductors at a first rate, and wherein said serializing the random pattern of bits comprises clocking the serial bit stream at a second rate equal to n times the first rate.

21. The method as recited in claim 19, wherein said generating comprises instructing a random bit generator to generate the random pattern of bits using instructions and an access port compatible with IEEE Std. 1149.1.

22. The method as recited in claim 19, wherein said comparing comprises forwarding a signal indicating functional failure status of the serializer and deserializer across an access port compatible with IEEE Std. 1149.1.